



H67H2-M3

Rev : 1.0

ECS CONFIDENTIAL

TABLE OF CONTENTS

Page	Index	Page	Index
1	Cover Page	26	IT8893(PCIE TO PCI)
2	Block Diagram	27	Slot - PCI1&PCI2
3	CPU - DMI/FDI/PEG	28	PCIE LAN RTL8111E/8105E
4	CPU - MISC	29	USB3.0 Etron EJ168 CONN
5	CPU - DDR3	30	Power Delivery
6	CPU - PWR/GND	31	Power Sequence, Reset Diagram
7	DDR3 - CH_A_DIMM1	32	Clock Distribution
8	DDR3 - CH_B_DIMM3		
9	VCore & VAXG-RT8859A		
10	VCore & VAXG- RT9616		
11	RT8121 DC/DC CPUVTT		
12	DC/DC VDIMM/DDR_VTT/5VDUAL		
13	Front Panel,FAN,PowerConn,GND,104		
14	PCH - DMI/PCI/PE/USB		
15	PCH - SATA / CLK		
16	PCH - MISC, Strap Function		
17	PCH - DP/VGA/FDI		
18	PCH - PWR		
19	PCH - GND		
20	Slot - PCI-EX16/PCI-EX1		
21	DVI&HDMI CONN&COM&PS2		
22	USB/SATA/SPI		
23	SIO-ITE8758E		
24	AUDIO VT1705/ALC662(CHIP)		
25	AUDIO VT1705/ALC662(PANEL)		

REVISION HISTORY:

Rev	Date	Notes
V.A	2010/05/20	Change from H67H2-M: 1. audio change to alc662/vt1705 2. 4"dimm change to 2"dimm 3. rear IO(PS2/HDMI co-lay DVI) 4. Super IO change to IT8758E
V.B	2010/08/10	Change from V.A: 1. Vcore co-lay RT8859M/Layout change VR12 ref GND 2. GP_V1.05 change to PCH 3. USB3.0 IC co-lay 3VSB 4. PCH change to QS 5. IT8893/EJ168 use Version:B 6. Add EZ charger circuit 7. BIOS ROM change to 32M
V.1.0	2010/10/11	Change from V.B: 1. EJ168 SMI to PCH for dos mode 2. power change as vendor 3. change IT8893 to CX 4. change HDMI ddc clk/data ESD to ESD-6P 5. Audio co-lay VT1705CE 6. change EN_6536 control for support decrease V_DIMM 7. change 25M cap to 22P for RTC

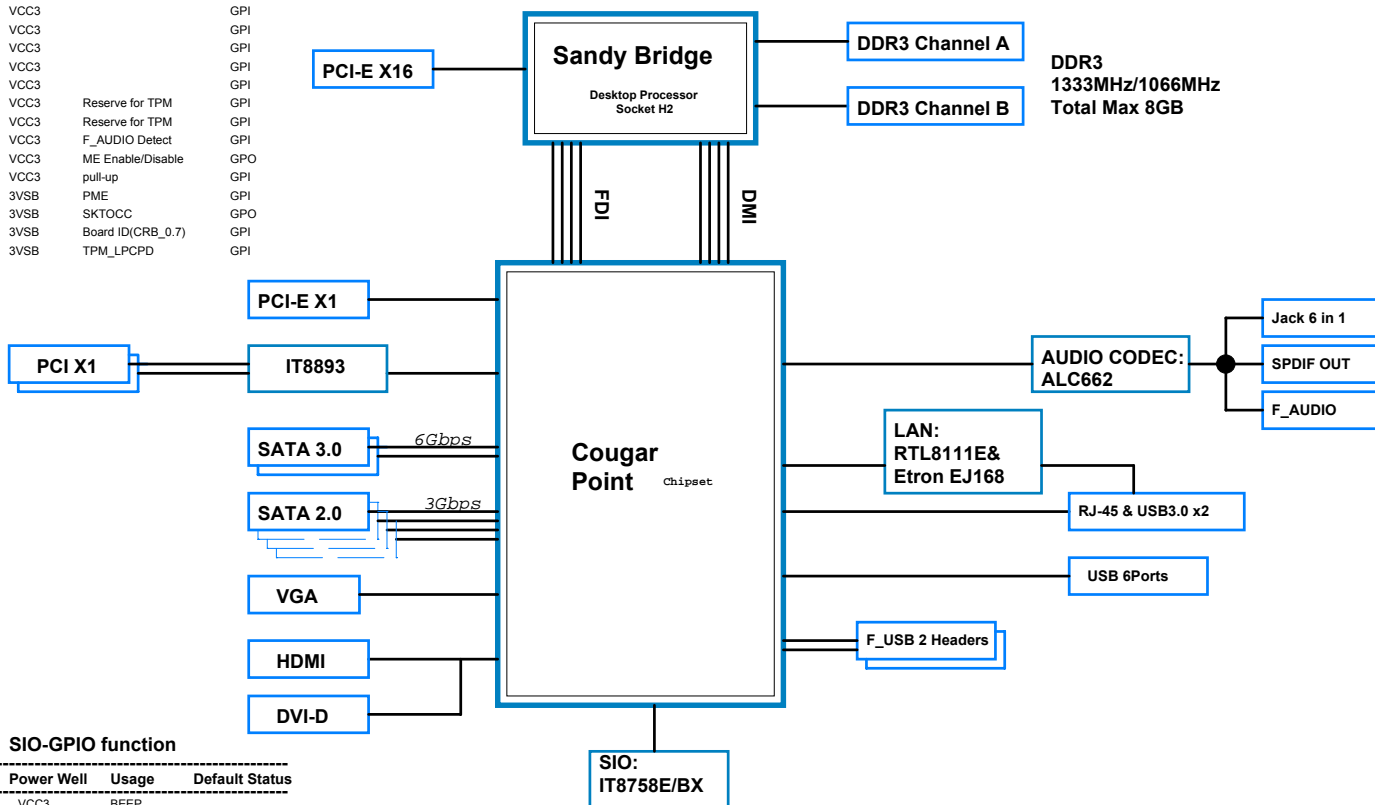
NOTE:
Design by 428971_Sugar_Bay_and_BromolowWS_PDG_Rev_0_8.pdf,
428880_428880_Cougar_Point_Desktop_Ballout_Mech_Package_Rev1p0.zip

Elitegroup Computer Systems

Title		Cover Page
Size	Document Number	H67H2-M3
Custom		Rev 1.0
Date	Monday, October 11, 2010	Sheet 1 of 32

PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3		GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO0	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI



SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	

Block Diagram			
File	Document Number	Rev	
Custom	H67H2-M3	1.0	
Date	Monday, October 11, 2010	Sheet	2 of 32

www.aitech1.ru

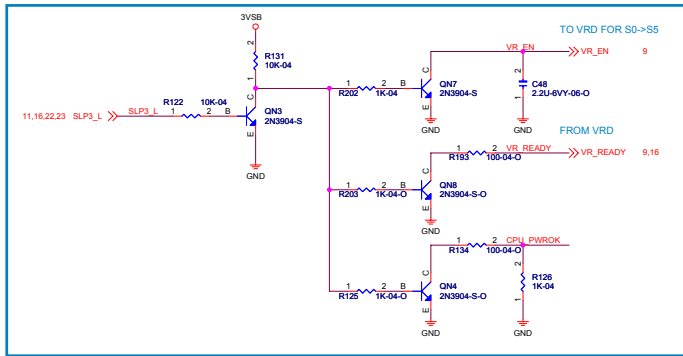
CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSALIBI, X1B
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	+	+	PECFGSEL[0]
6	+	+	PECFGSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG_0..17 HAVE INTERNAL PULL-UPS

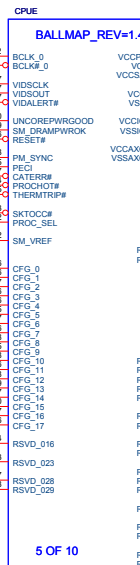
PCIE CONFIG	SELO	SEL1
1 X 16	1	1
2 X 8	0	1

CFG[5:6]:
11=DEFAULT X16,
01=X8,
10=RESERVED,
00=X8,X4,X4

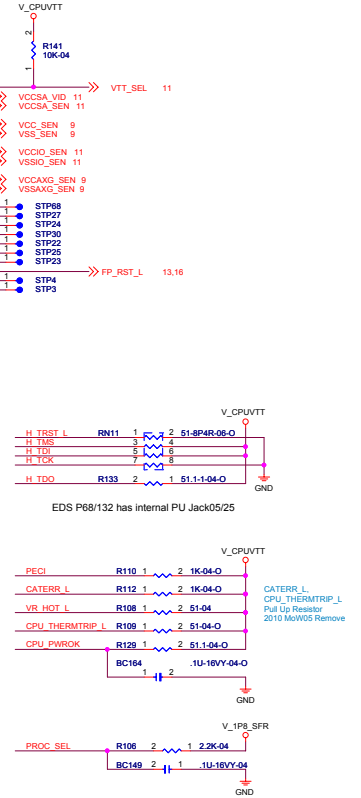
Power Down Sequencing Circuit



change test point for internal PU Jack05/25



5 OF 10

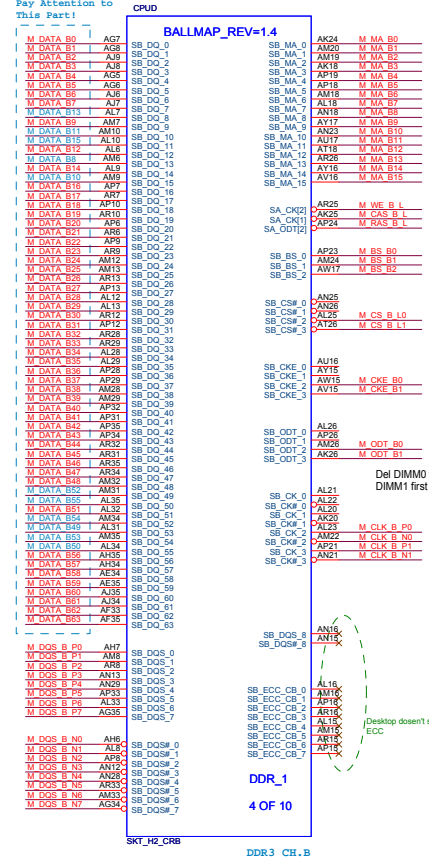
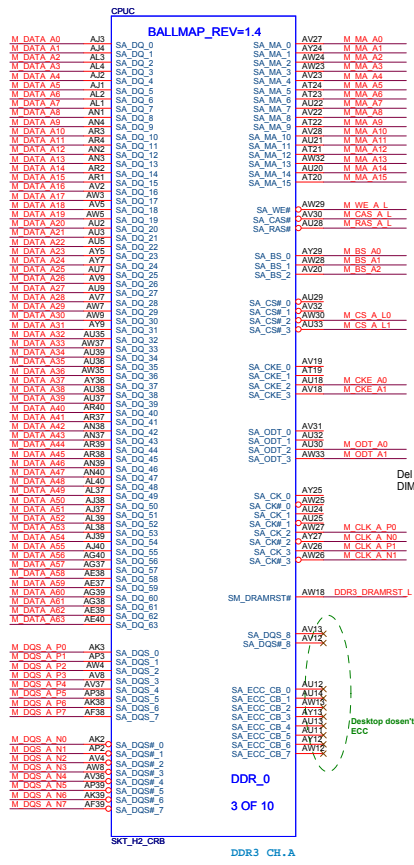
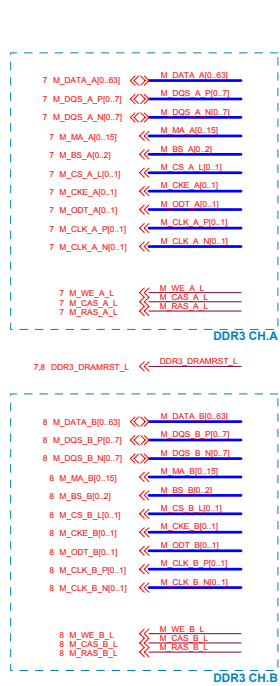


EDS P68/132 has internal PU Jack05/25

DMI/FDI termination voltage:
DC coupled: TX/RX to VCC ISF sampled high
DC coupled: TX/RX TO VSS IF sampled low
AC COUPLED: TX set to VCC/2, RX set to VSS regardless of this strap

Elitegroup Computer Systems

CPU - MISC	
Docu	Document Number
H67H2-M3	
Date:	Monday, October 11, 2010
Sheet	4 of 92



Elitegroup Computer Systems

Rev: CPU - DDR3

Document Number: H67H2-M3

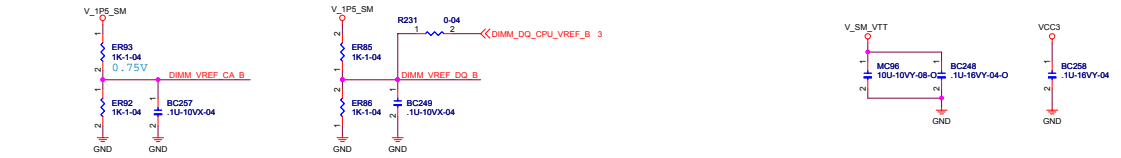
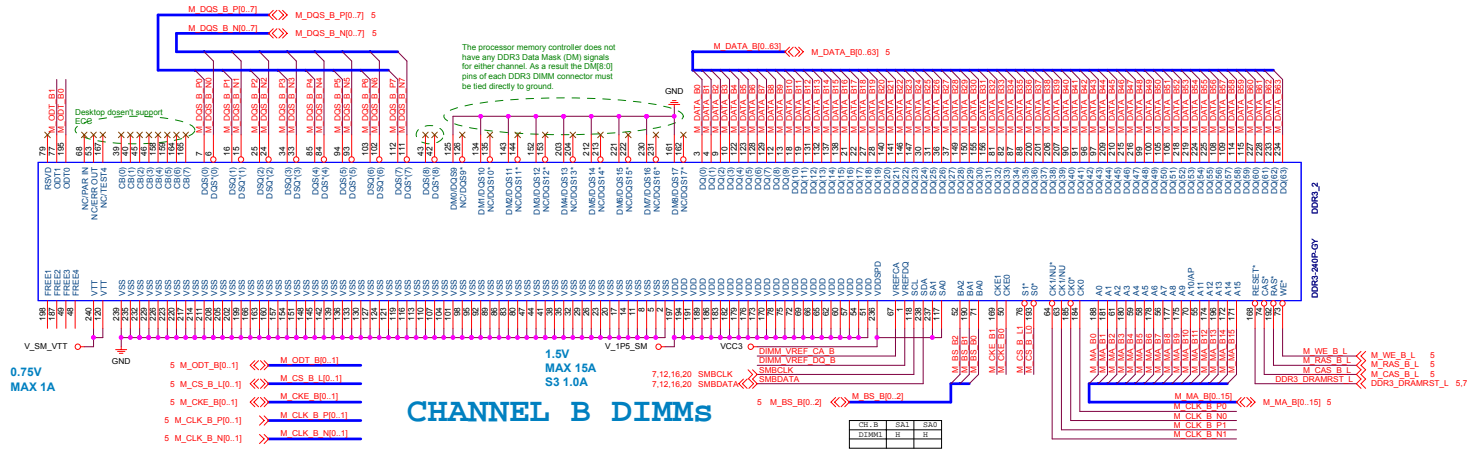
Date: Monday, October 11, 2010

Sheet: 5 of 92

Rev: 1.0

www.aitech1.ru



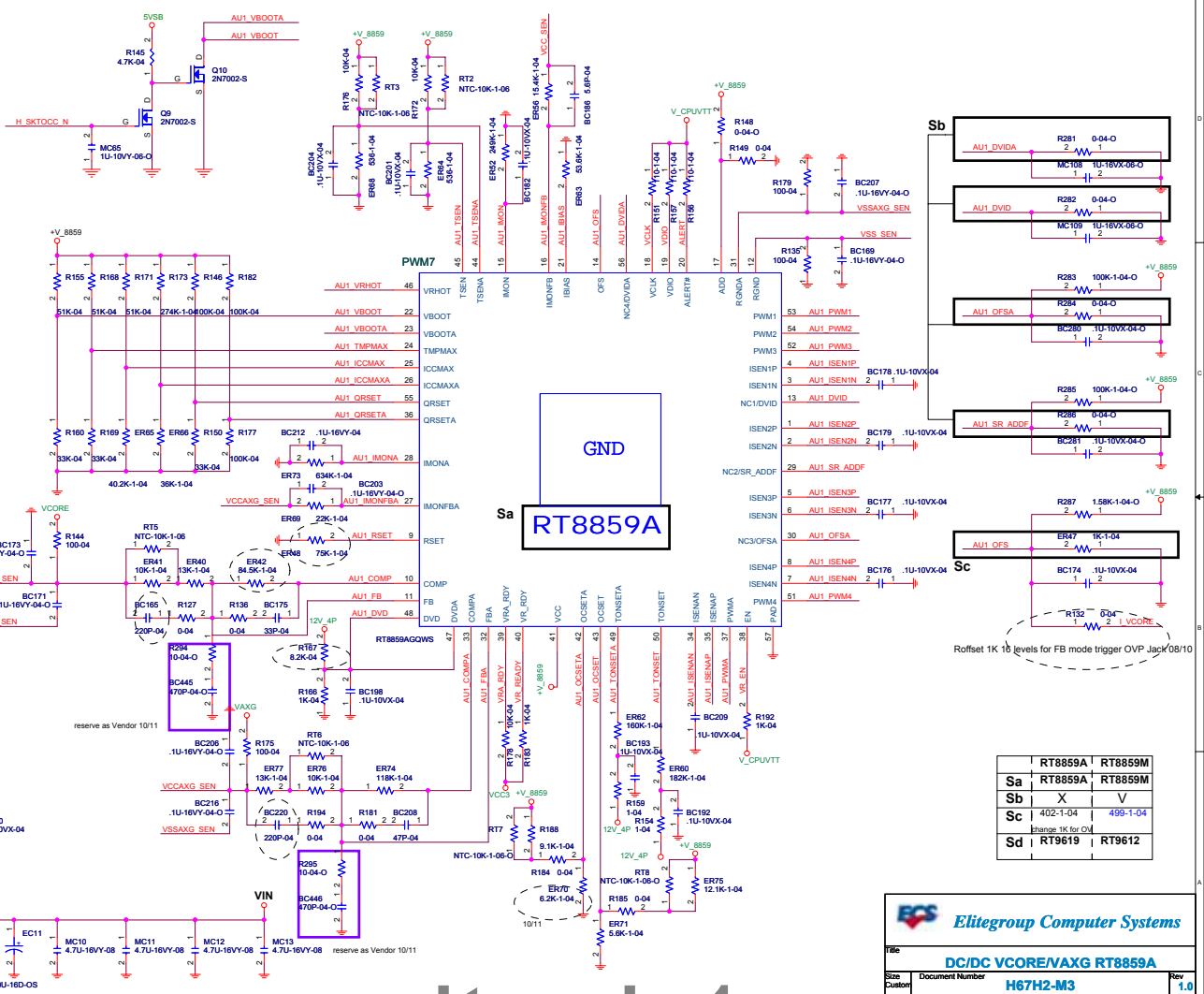
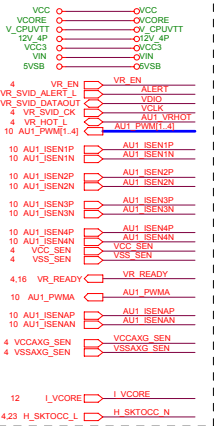


Del DIMM3 for always populate DIMM4 first Jack 05/13

File		DDR3 - CH_B_DIMM3	
Size	Document Number	H67H2-M3	
Custom			
Date	Monday, October 11, 2010	Sheet	8 of 92
		Rev	1.0

www.aitech1.ru

External Connection



	RT8859A	RT8859M
Sa	RT8859A	RT8859M
Sb	X	V
Sc	402-1-04	499-1-04
Sd	RT9619	RT9612

Elitegroup Computer Systems

File: **DC/DC VCC/VAXG RT8859A**

Size: Document Number **H67H2-M3**

Date: Monday, December 20, 2010

Sheet: 8 of 92

Rev: 1.0

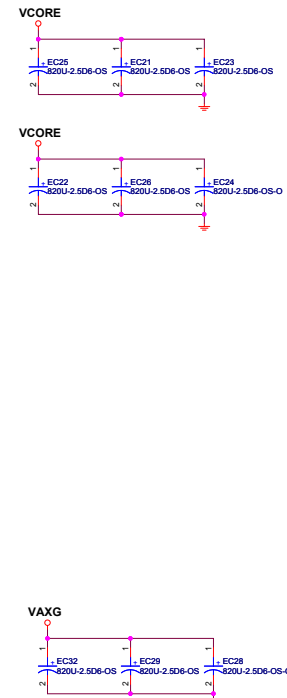
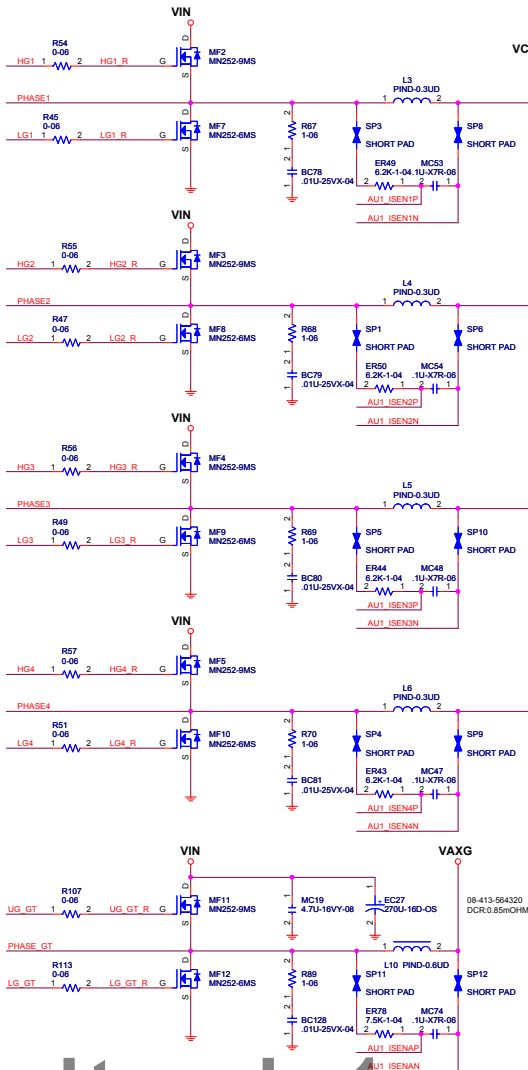
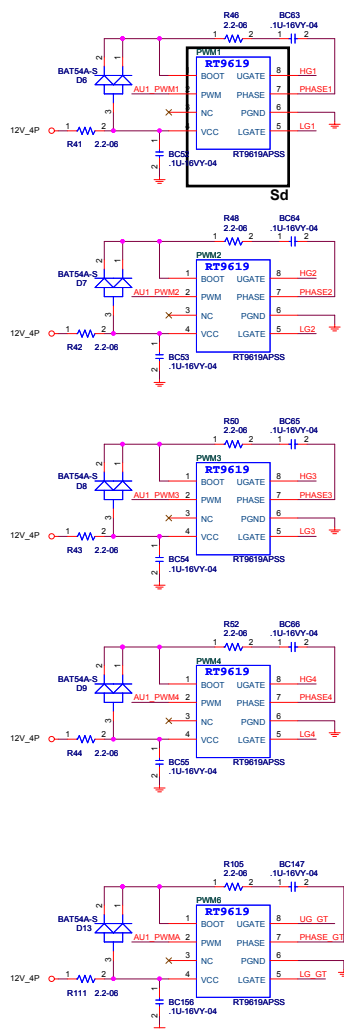
www.aitech1.ru

External Connection

VCC	0-06	0-06
VCCORE	0-06	0-06
12V_4P	0-06	0-06
VCC3	0-06	0-06
VIN	0-06	0-06

9 AU1_PWM1_4	AU1_PWM1_4
9 AU1_ISEN1P	AU1_ISEN1P
9 AU1_ISEN1N	AU1_ISEN1N
9 AU1_ISEN2P	AU1_ISEN2P
9 AU1_ISEN2N	AU1_ISEN2N
9 AU1_ISEN3P	AU1_ISEN3P
9 AU1_ISEN3N	AU1_ISEN3N
9 AU1_ISEN4P	AU1_ISEN4P
9 AU1_ISEN4N	AU1_ISEN4N
4.9 VCC_SEN	VCC_SEN
4.9 VSS_SEN	VSS_SEN

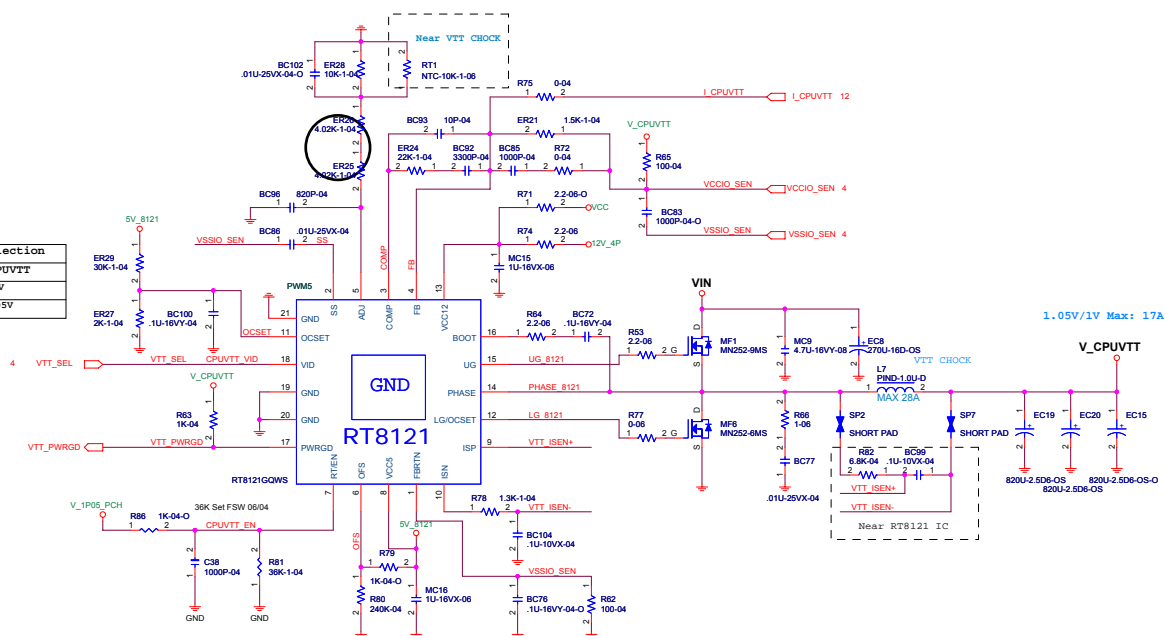
9 AU1_PWM2	AU1_PWM2
9 AU1_ISEN2P	AU1_ISEN2P
9 AU1_ISEN2N	AU1_ISEN2N
9 AU1_ISEN3P	AU1_ISEN3P
9 AU1_ISEN3N	AU1_ISEN3N
9 AU1_ISEN4P	AU1_ISEN4P
9 AU1_ISEN4N	AU1_ISEN4N
4.9 VCC_SEN	VCC_SEN
4.9 VSS_SEN	VSS_SEN



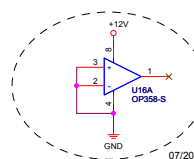
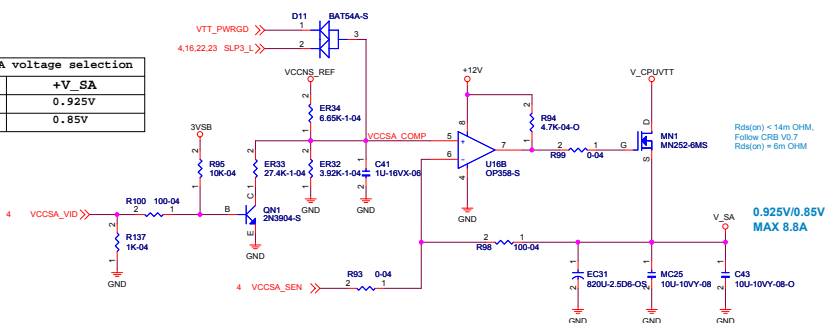
Elitegroup Computer Systems			
File	DC/DC VCCORE/VAXG RT9619		
Size	Document Number	H67H2-M3	
Custom		Rev 1.0	
Date	Monday, December 20, 2010	Sheet	10 of 32

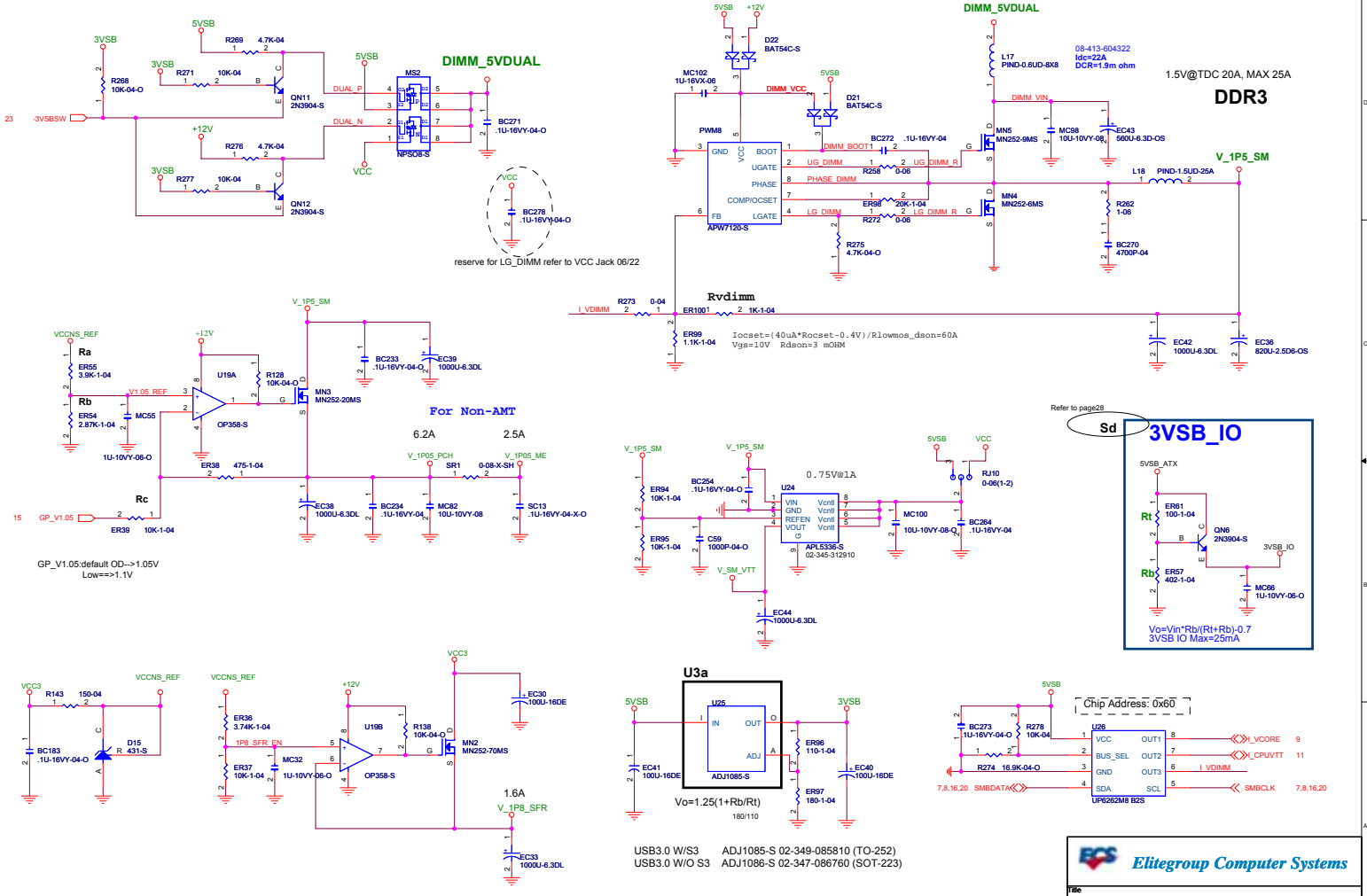
www.aitech1.ru

VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V

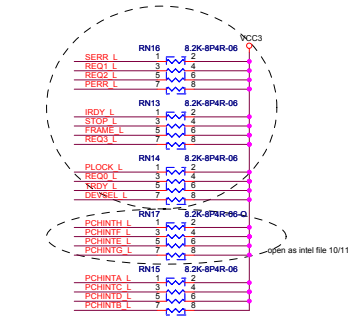
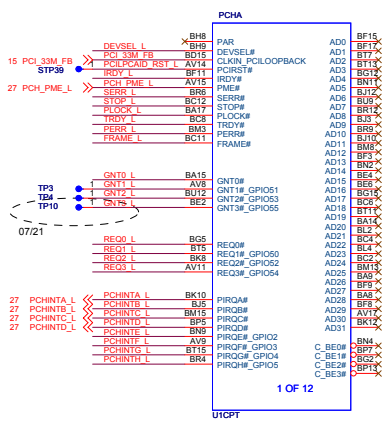


VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V





www.aitech1.ru

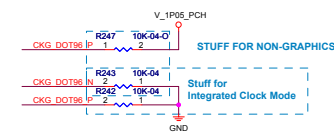


GNT[0..3]#
GPIO19
Have been internal pull high to +VCC3

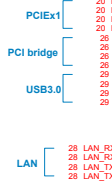
Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

GPIO19:
Boot Device Select Strap.
GNT0_L:
No More Information in EDS V0.7
GNT1_L:
Boot Device Select Strap.
GNT2_L:
ES1 Strap (Server Only).
DON'T Pull Low in Desktop.
GNT3_L:
Top-Block Swap Override Mode.
When Sampled Low.



For H61:PCIE 7/8 is disable...From intel Jasmine



For H61:USB 6/7/2/3 is disable...From 440377 file

GPIO19:
Boot Device Select Strap.

GNT0_L:
No More Information in EDS V0.7

GNT1_L:
Boot Device Select Strap.

GNT2_L:
ES1 Strap (Server Only).
DON'T Pull Low in Desktop.

GNT3_L:
Top-Block Swap Override Mode.
When Sampled Low.

GNT[0..3]#
GPIO19
Have been internal pull high to +VCC3

Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

GPIO19:
Boot Device Select Strap.

GNT0_L:
No More Information in EDS V0.7

GNT1_L:
Boot Device Select Strap.

GNT2_L:
ES1 Strap (Server Only).
DON'T Pull Low in Desktop.

GNT3_L:
Top-Block Swap Override Mode.
When Sampled Low.

GNT[0..3]#
GPIO19
Have been internal pull high to +VCC3

Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

GPIO19:
Boot Device Select Strap.

GNT0_L:
No More Information in EDS V0.7

GNT1_L:
Boot Device Select Strap.

GNT2_L:
ES1 Strap (Server Only).
DON'T Pull Low in Desktop.

GNT3_L:
Top-Block Swap Override Mode.
When Sampled Low.

GNT[0..3]#
GPIO19
Have been internal pull high to +VCC3

Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

GPIO19:
Boot Device Select Strap.

GNT0_L:
No More Information in EDS V0.7

GNT1_L:
Boot Device Select Strap.

GNT2_L:
ES1 Strap (Server Only).
DON'T Pull Low in Desktop.

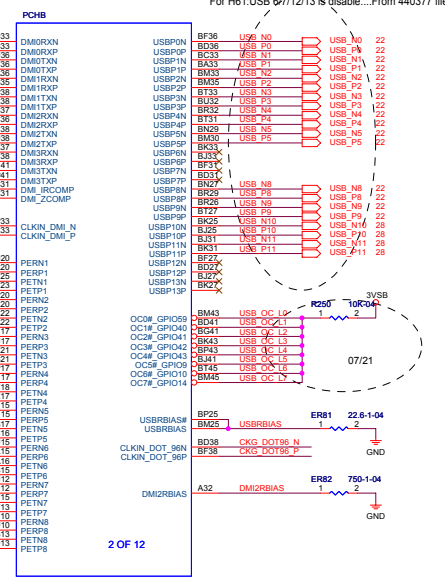
GNT3_L:
Top-Block Swap Override Mode.
When Sampled Low.

GNT[0..3]#
GPIO19
Have been internal pull high to +VCC3

Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

GPIO19:
Boot Device Select Strap.



GPIO19:
Boot Device Select Strap.

GNT0_L:
No More Information in EDS V0.7

GNT1_L:
Boot Device Select Strap.

GNT2_L:
ES1 Strap (Server Only).
DON'T Pull Low in Desktop.

GNT3_L:
Top-Block Swap Override Mode.
When Sampled Low.

GNT[0..3]#
GPIO19
Have been internal pull high to +VCC3

Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

GPIO19:
Boot Device Select Strap.

GNT0_L:
No More Information in EDS V0.7

GNT1_L:
Boot Device Select Strap.

GNT2_L:
ES1 Strap (Server Only).
DON'T Pull Low in Desktop.

GNT3_L:
Top-Block Swap Override Mode.
When Sampled Low.

GNT[0..3]#
GPIO19
Have been internal pull high to +VCC3

Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

GPIO19:
Boot Device Select Strap.

GNT0_L:
No More Information in EDS V0.7

GNT1_L:
Boot Device Select Strap.

GNT2_L:
ES1 Strap (Server Only).
DON'T Pull Low in Desktop.

GNT3_L:
Top-Block Swap Override Mode.
When Sampled Low.

GNT[0..3]#
GPIO19
Have been internal pull high to +VCC3

Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

GPIO19:
Boot Device Select Strap.

GNT0_L:
No More Information in EDS V0.7

GNT1_L:
Boot Device Select Strap.

GNT2_L:
ES1 Strap (Server Only).
DON'T Pull Low in Desktop.

GNT3_L:
Top-Block Swap Override Mode.
When Sampled Low.

GNT[0..3]#
GPIO19
Have been internal pull high to +VCC3

Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

GPIO19:
Boot Device Select Strap.

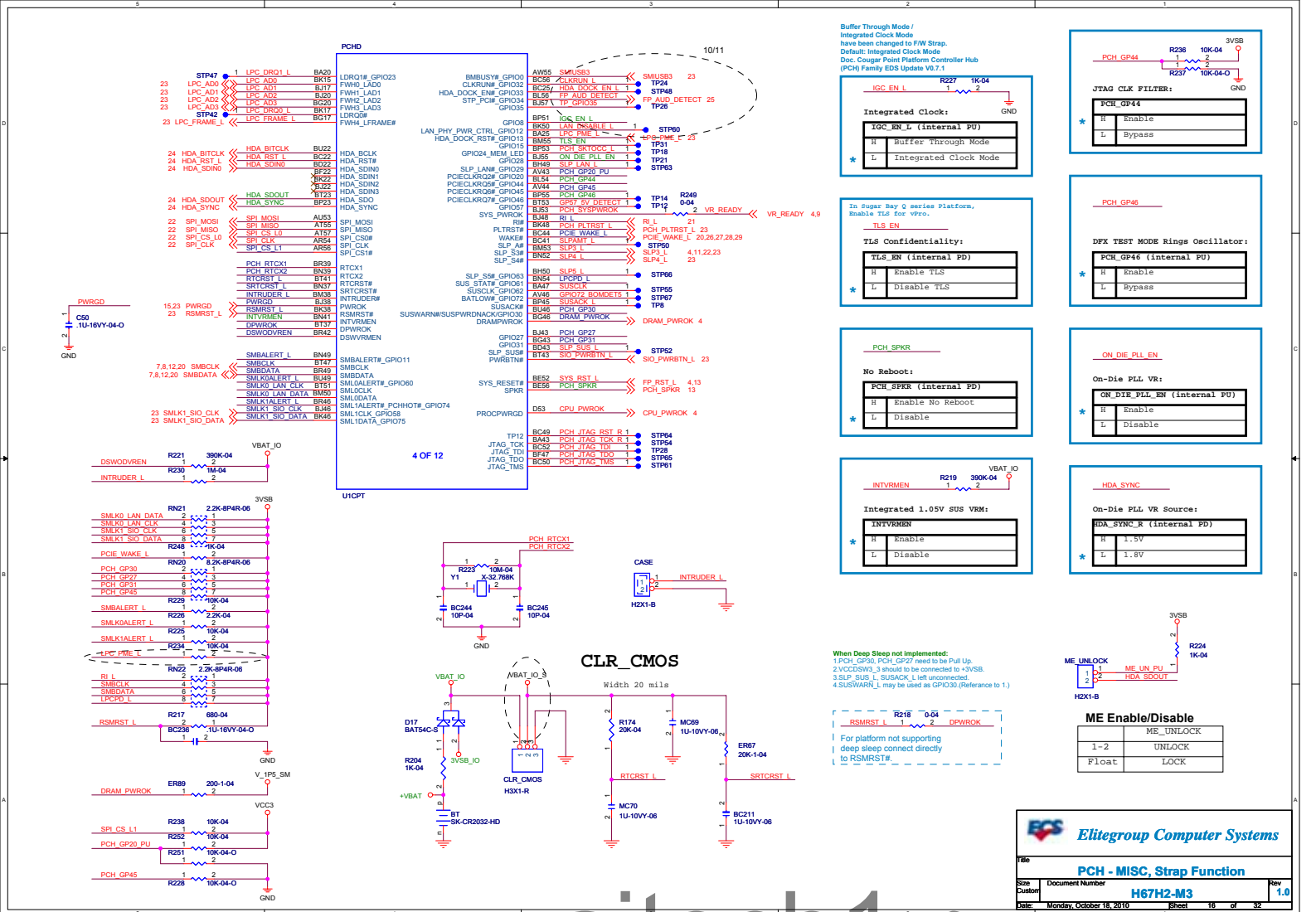
Elitegroup Computer Systems

File: PCH - DMI/PCI/PE/USB

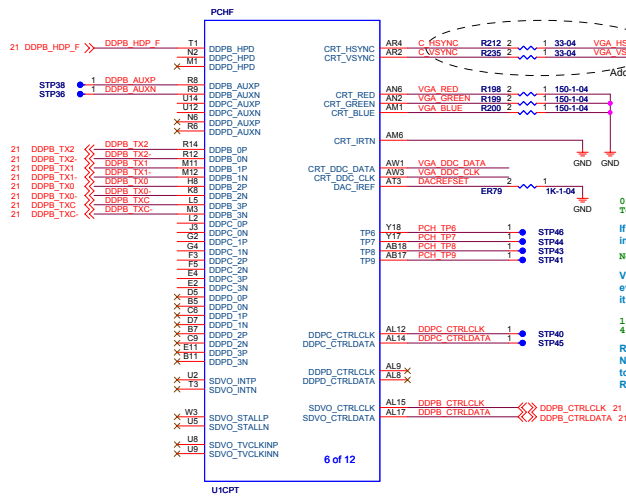
Size: Document Number H67H2-M3

Date: Monday, October 18, 2010 Sheet 14 of 32

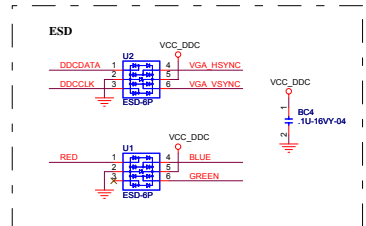
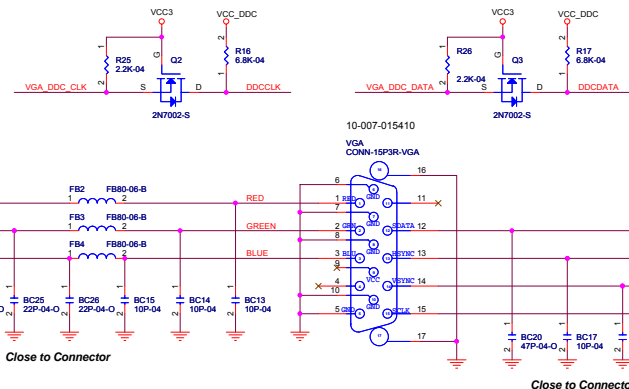
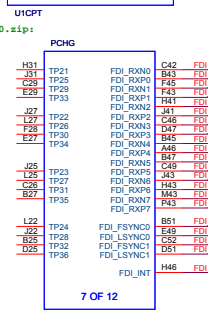
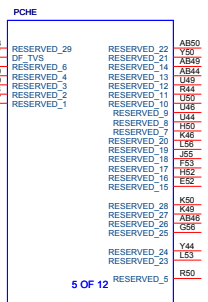




www.aitech1.ru



091222 Update!
Terminating unused DC NAND interface:
If not implemented, the dual channel NAND interface signals, including NV_RCOMP, can be left as No Connect.
Note:
VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.
100120 Update!
428880, 428880, Cougar_Point_Desktop_Ballout_Mech_Package_Rev1p0.zip:
Renamed NV_WE#_CK[0:1], NV_RE#_WRB[0:1], NV_RCOMP, NV_RB#, NV_DQS / NV_IO[0:15], NV_DQS[0:1], NV_CE#[0:3], and NV_ALE to Reserved(RSVD).
Renamed NV_CLE to DF_TV5.



Elitegroup Computer Systems

PCH - DP/VGA/FDI


Size: Document Number: H67H2-M3

Date: Monday, October 11, 2010 Sheet: 17 of 32

Rev: 1.0

www.aitech1.ru



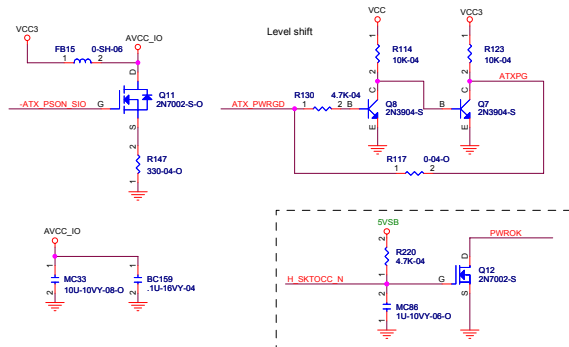
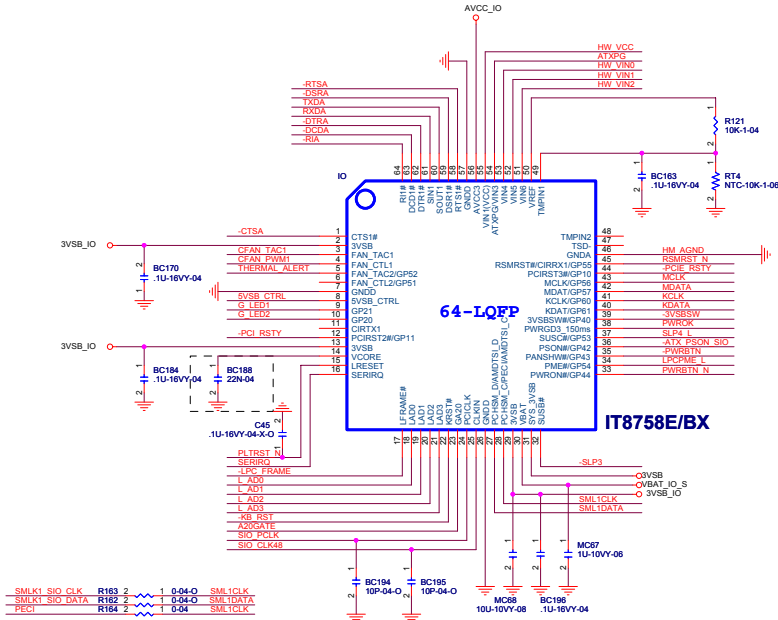
 Elitegroup Computer Systems			
Title			
Slot - PCI-EX16/PCI-EX1			
Size	Document Number	Rev	
Custom	H67H2-M3	1.0	
Date:	Monday, October 11, 2010	Sheet	20 of 32



16	IVSBO	OV3SB	
	OV5BO	OV5SB	
	VOC	OVOC3	
	VBAT_IO_S	OVBAT_IO_S	
	OVCC	OVCC	
	V_1P5_S	OV_1P5_S	
	VP_CUVIT1	OV_CUVIT1	
	VOORE	OVORE	
16	LPC_PME_L	LPCPME_L	
16	LPC_FRAME_L	LPC_FRAME	
16	LPC_ADI0_[3]	LAD0_3	LPC
16	RSMRST_L	RSMRST_N	
13	FP_PWBRTN_L	PWBRTN	
16	FP_PWBRTN_L	PWBRTN_N	
16	SLP_L	SLP	
16	SLP_L1	SLP_L1	
13	PSRON_L	ATX_PSRON_SIO	
13	ATX_PWRGD	PWRGD	
15,16	PWRGD	PWRKR	
16	PCH_PLTRST_L	PLTRST_N	
20	SIO_PDIRST_L	PDIRST	
28,29	SIO_PDIRST_L	PDIRST_RSTY	
15	KBRST_L	KB_RST	
15	AD2STATE	AD2STATE	
15	SERIO	SERIRQ	
12	SVSSWB	SVSSWB	
13	CFAN_TAC1	CFAN_TAC1	
13	CFAN_PWM1	CFAN_PWM1	
15	SIO3SM	SIO_CLK4	
15	SIO4M1	SIO_CLK4B	
13	G_LED1	G_LED1	
13	G_LED2	G_LED2	
21	KLCK	KLCK	
21	KDATA	KDATA	
21	MDCL	MDCL	
21	MDATA	MDATA	
16	SMKL1_SIO_CLK	SMKL1_SIO_CLK	
16	SMKL1_SIO_DATA	SMKL1_SIO_DATA	
14,15	PEC1	PEC1	
4,9	H_SKTCC2	H_SKTCC2_N	
	Thermal Alert	Thermal Alert	
22	SVSB_CTRL	SVSB_CTRL	

21	-RIA	21	-RIA
21	-DTRA	21	-DTRA
21	-CTSA	21	-CTSA
21	TXDA	21	TXDA
21	-RTSA	21	-RTSA
21	RXDA	21	RXDA
21	-DSRA	21	-DSRA
21	-DCDA	21	-DCDA

FJP1 & FJP2 Pin 60& 23	FAN_CTL_SEL	11	The default value of EC Index 63h/6Bh/73h is 80h (50%)
		10	The default value of EC Index 63h/6Bh/73h is FFh(Fan off)
		01	The default value of EC Index 63h/6Bh/73h is 00h(Fan full speed)
		00	The default value of EC Index 63h/6Bh/73h is 40h



The schematic diagram shows four power supply rails for the ADXL345: HW_VCC, HW_VIN0, HW_VIN1, and HW_VIN2. Each rail is connected to a 1U-18V-04-0 voltage regulator. The regulators are connected to the VCC, VCCORE, V1PS_SMI, and CPLV_VTT pins of the ADXL345. The regulators are connected to the VCC, VCCORE, V1PS_SMI, and CPLV_VTT pins of the ADXL345. The regulators are connected to the VCC, VCCORE, V1PS_SMI, and CPLV_VTT pins of the ADXL345.

Note:
Most pull-ups are provided

Sa

ATX_PSON_SIO
PWREN

RJ3 4.7K-04(1-2)

2 1
3 2
4 3

RJ4 4.7K-04(1-2)

2 1
3 2
4 3

3V5S_I/O
5VS5

VCC3

PWROK R142 2 10K-04

CFAN_TAC1 BC172 1 470P-0-0

Sb

3VSB — 2 — 1 — 3VSB_IO
R165 0-08-0
5VSB — 1 — 2 — 5VSB_ATX
R263 0-08-0

	2-3	1-
Sa	V	X
Sb	X	V
Sc	X	V
Sd	X	V

page 11

[illegible]

Title			
SIO-ITE8758E			
Size	Document Number	Rev	
Custom	H67H2-M3	1.0	
Date:	Monday, October 11, 2010	Sheet	23 of 32

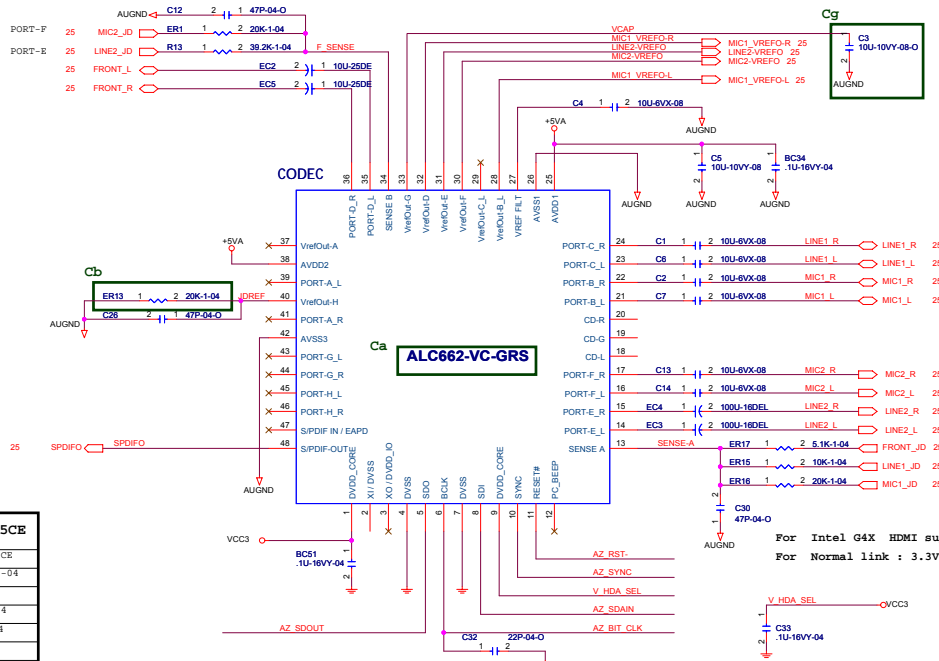
External Connection

5VSB → 5VSB
VCC → VCC
+12V → +12V
VCC3 → VCC3

16 HDA_RST_L → AZ_RST-
16 HDA_BITCLK → AZ_BIT_CLK
16 HDA_SYNC → AZ_SYNC
16 HDA_SDIN → AZ_SDIN
16 HDA_SDOUT → AZ_SDOUT

AGND → AGND

* VCC1.5 can remove for non-Intel G4X platform



BOM Difference

Location	ALC662	VT1705	VT1705CE
Ca	ALC662-VC-GRS	VT1705	VT1705CE
Cb	20K-1-04	5.1K-1-04	5.1K-1-04
Cc	V	X	X
Cd	2.2K-04	3.3K-04	3.3K-04
Ce	75-04	75-04	75-04
Cf	X	X	V
Cg	X	X	V
Ch	V	V	X

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

Elitegroup Computer Systems

File	AUDIO VT1705/ALC662 (CHIP)		
Size	Document Number	H67H2-M3	Rev 1.0
Custom			
Date	Monday, October 11, 2010	Sheet	24 of 32

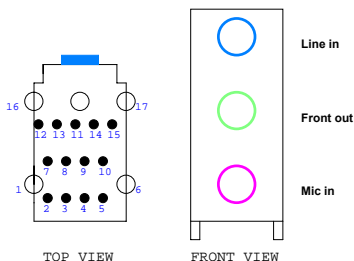
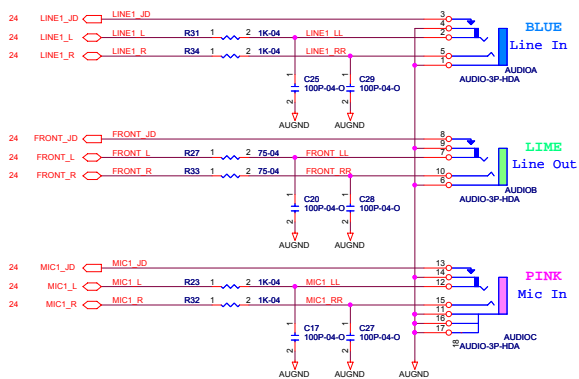
www.aitech1.ru

External Connection

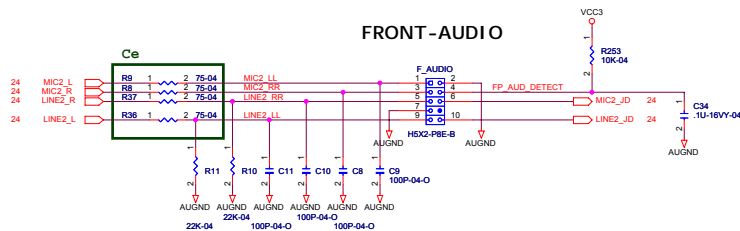
16 FP_AUD_DETECT ← FP_AUD_DETECT

* HDPANEL_DETECT connect to SIO or SB GPIO for AC97 Panel support

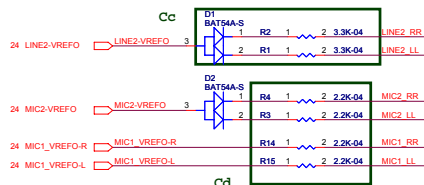
REAR-AUDIO Non re-tasking for rear panel



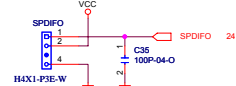
FRONT-AUDIO



MIC Bias



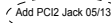
SPDIF-OUT



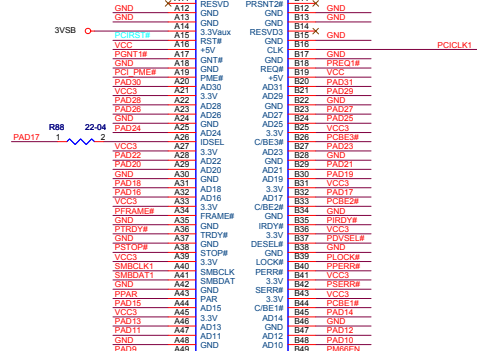
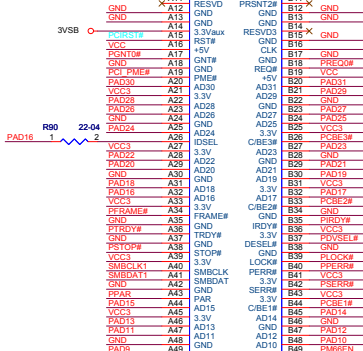
AUDIO VT1705/ALC662 (PANEL)			
File	Document Number	Rev	1.0
Size	Custom	H67H2-M3	
Date	Monday, October 11, 2010	Sheet	25 of 32

www.aitech1.ru

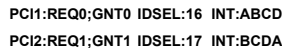
✓ Add PCI2 Jack 05/13



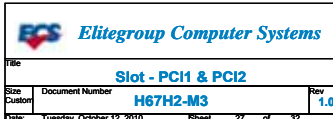
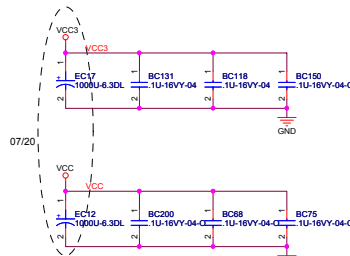
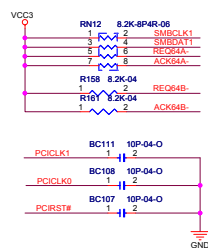
PCI 2



PCI1:REQ0;GNT0 IDSEL:16 INT:ABCD
PCI2:REQ1;GNT1 IDSEL:17 INT:BCDA

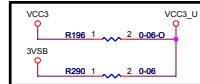


As document WW32 2010 Sandy Bridge and Cougar Point Based Platforms Field Message of the Week



External Connection

U3b

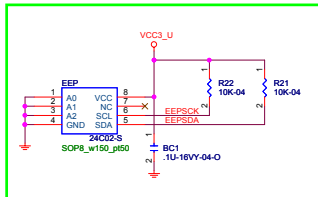
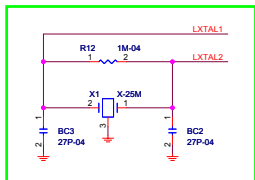
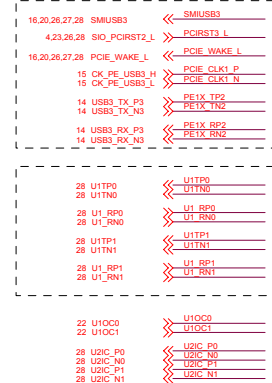
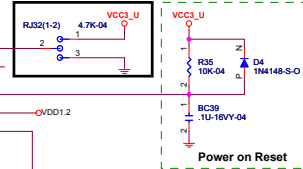


USB3.0 w/o s3	USB3.0 w s3
U3a	1086
U3b	1085
U3c	X
U3d	ER18
U3e	2-3

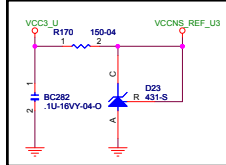
W1a



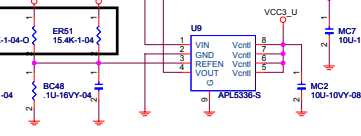
U3e



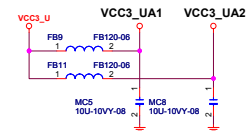
U3c



U3d



	W/USB3.0	W/O USB3.0
W1a	V	V page 29 but W1a
W1b	V	X
W1c	1-2	2-3
W1d	V	X
W1e	X	V
W1f	V	X
W1g	install as Conn/ESD require	



Elitegroup Computer Systems

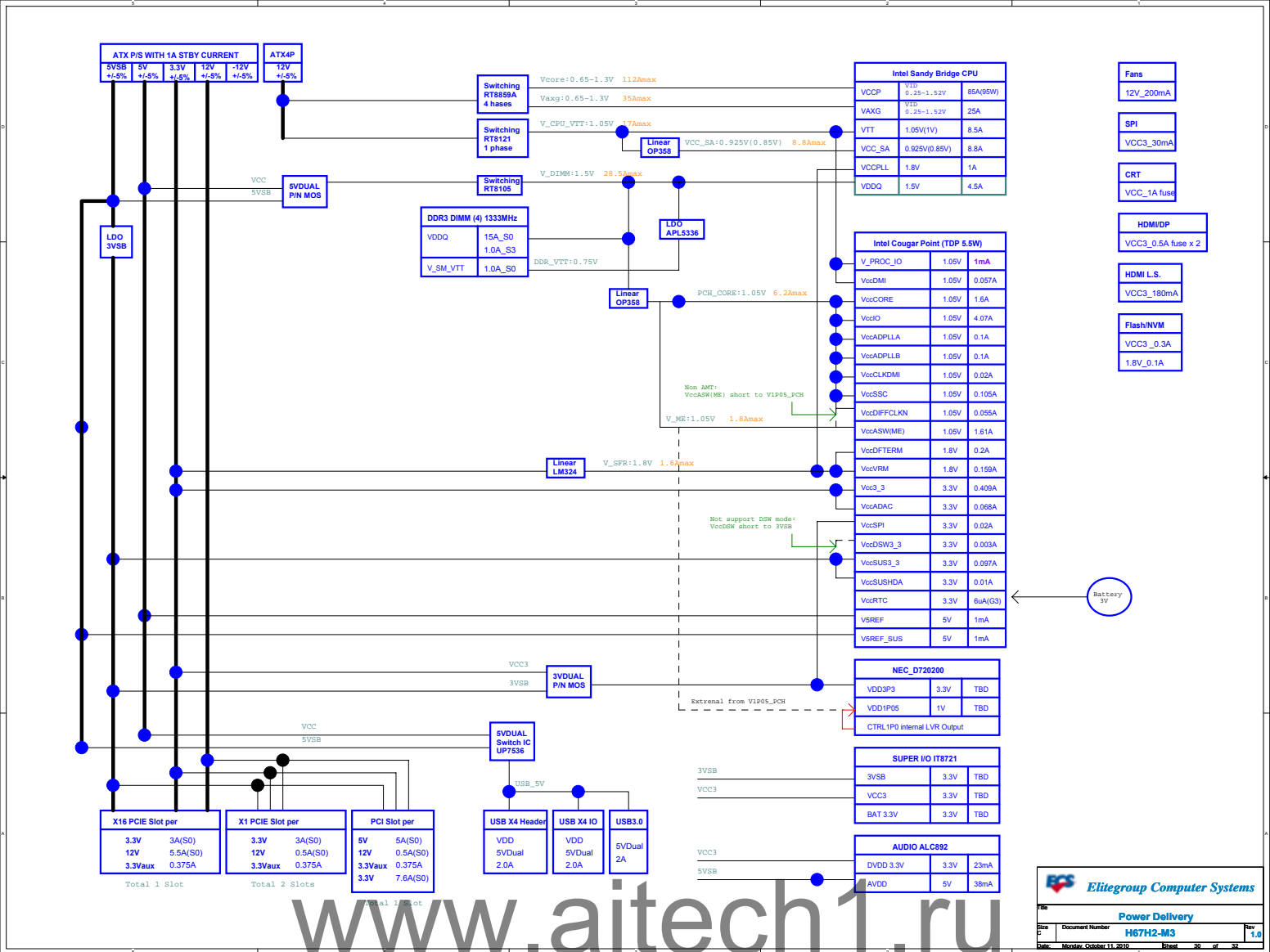
File: **USB3.0 Etron EJ168 CONN**

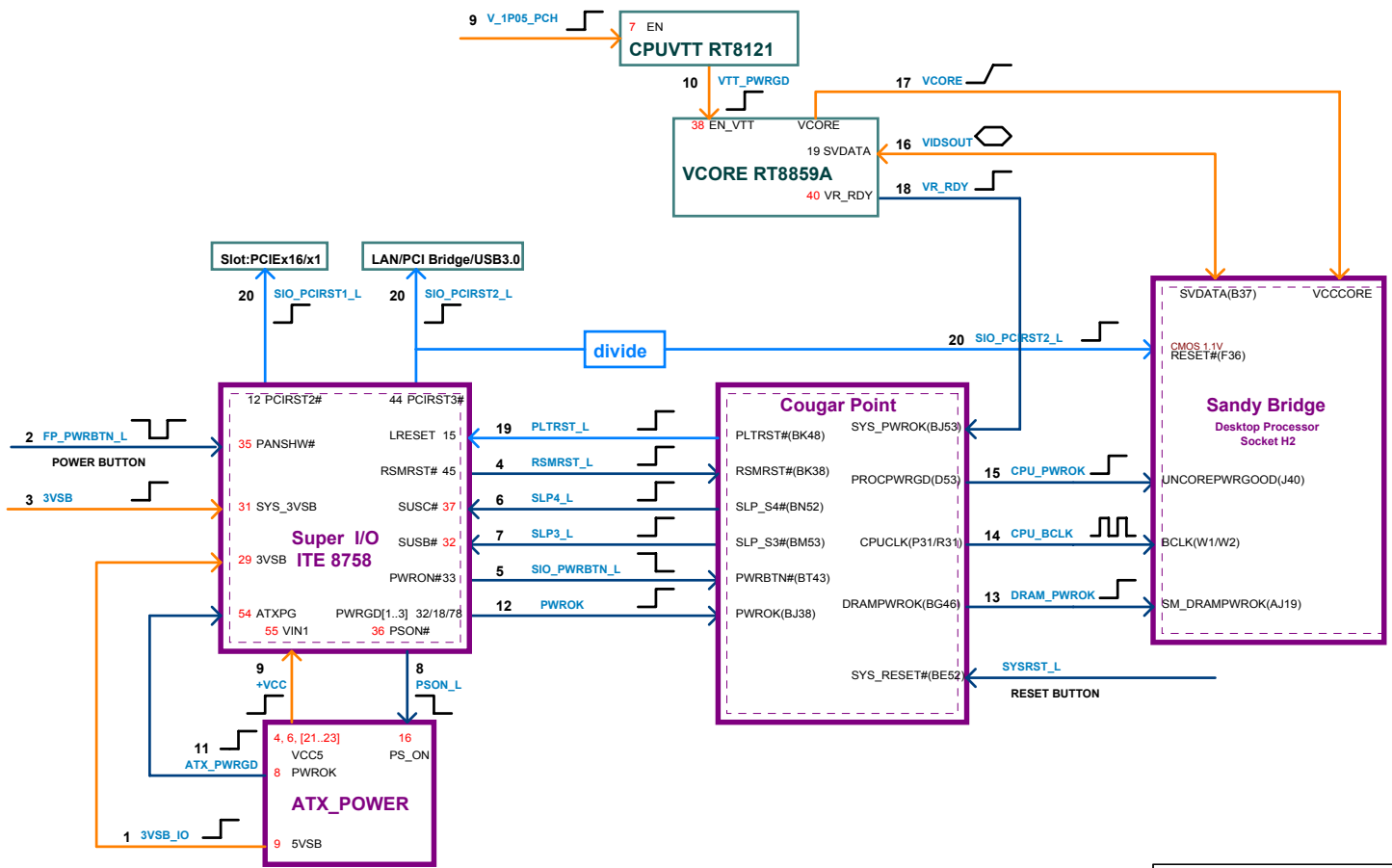
Size: Document Number **H67H2-M3**

Custom: **Rev 1.0**

Date: Wednesday, October 20, 2010 Sheet 29 of 32

www.aitech1.ru



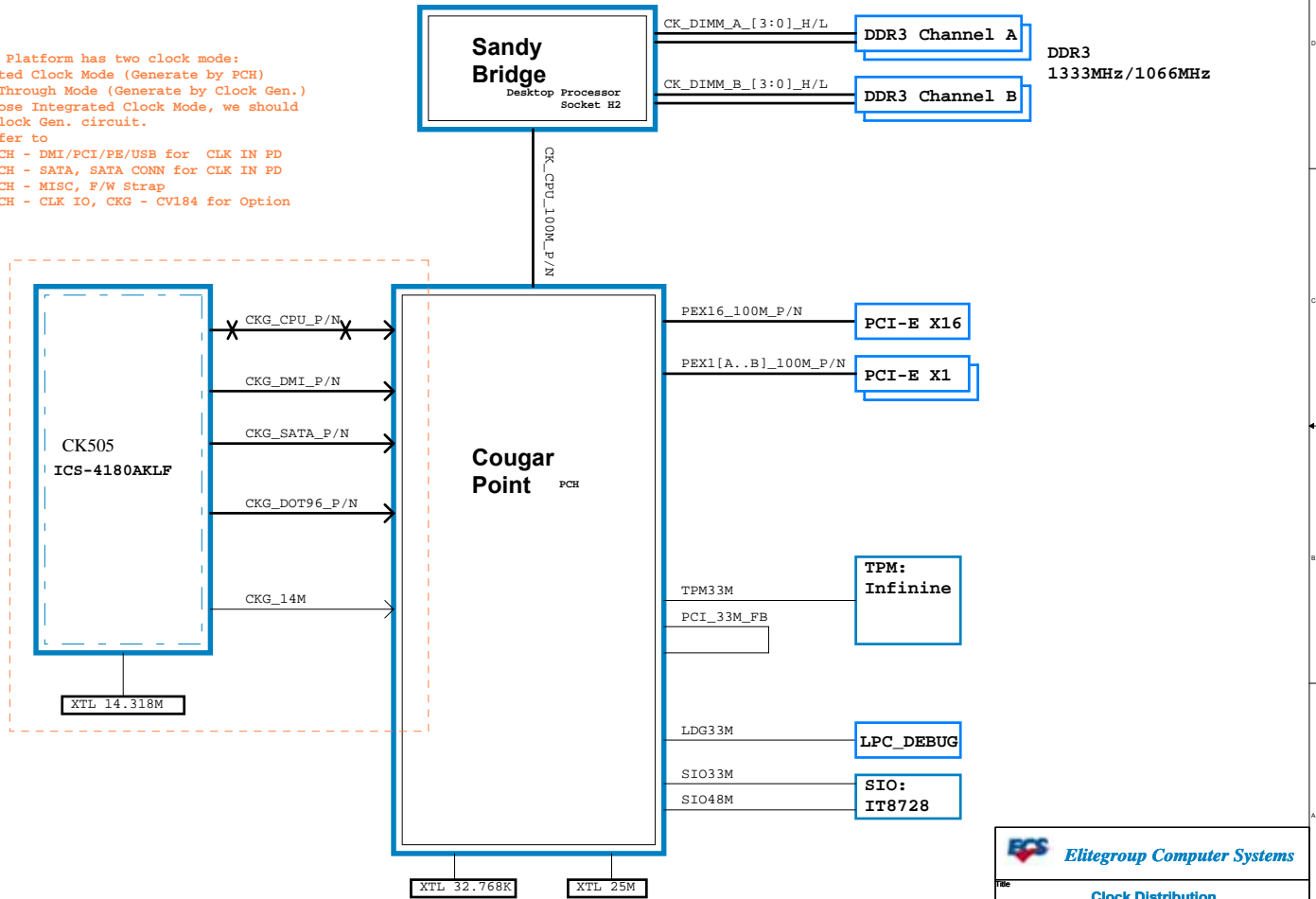



Power Sequence, Reset Diagram			
File	Document Number	Rev	1.0
Size	Custom	H67H2-M3	
Date	Monday, October 11, 2010	Sheet	31 of 32

www.aitech1.ru

NOTE:

Sugar Bay Platform has two clock mode:
1.Integrated Clock Mode (Generate by PCH)
2.Buffer Through Mode (Generate by Clock Gen.)
If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.
Please refer to
Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD
Page.13 PCH - SATA, SATA CONN for CLK IN PD
Page.14 PCH - MISC, F/W Strap
Page.15 PCH - CLK IO, CKG - CV184 for Option



 Elitegroup Computer Systems			
Title: Clock Distribution			
Size: Custom	Document Number: H67H2-M3	Rev: 1.0	
Date: Monday, October 11, 2010	Sheet: 32	of: 32	

www.aitech1.ru